

TDA9935

Dual 14-bit, up to 160 Msample/s, 2 × interpolating Digital-to-Analog Converter (DAC)

Rev. 04 — 17 September 2007

Product data sheet

1. General description

The TDA9935 is optimized to reduce architecture complexity and overall system cost. Thanks to its direct IF conversion capabilities, it leads dynamic performance in multi-carrier support. With an internal sampling rate up to 160 Msample/s, TDA9935 is an extremely competitive solution for WCDMA, CDMA2000 and GSM/EDGE transmitters, as well as high data rate radio services like WLL, LMDS and BWA.

2. Features

- Dual 14-bit resolution
- SFDR = 80 dBc at 2.5 MHz
- Input data rate up to 80 Msample/s
- 2 × interpolation filter
- Output data rate up to 160 Msample/s
- Single 3.3 V power supply
- Low noise capacitor-free integrated PLL
- Low power dissipation
- HTQFP80 package
- Ambient temperature from -40 °C to +85 °C

3. Applications

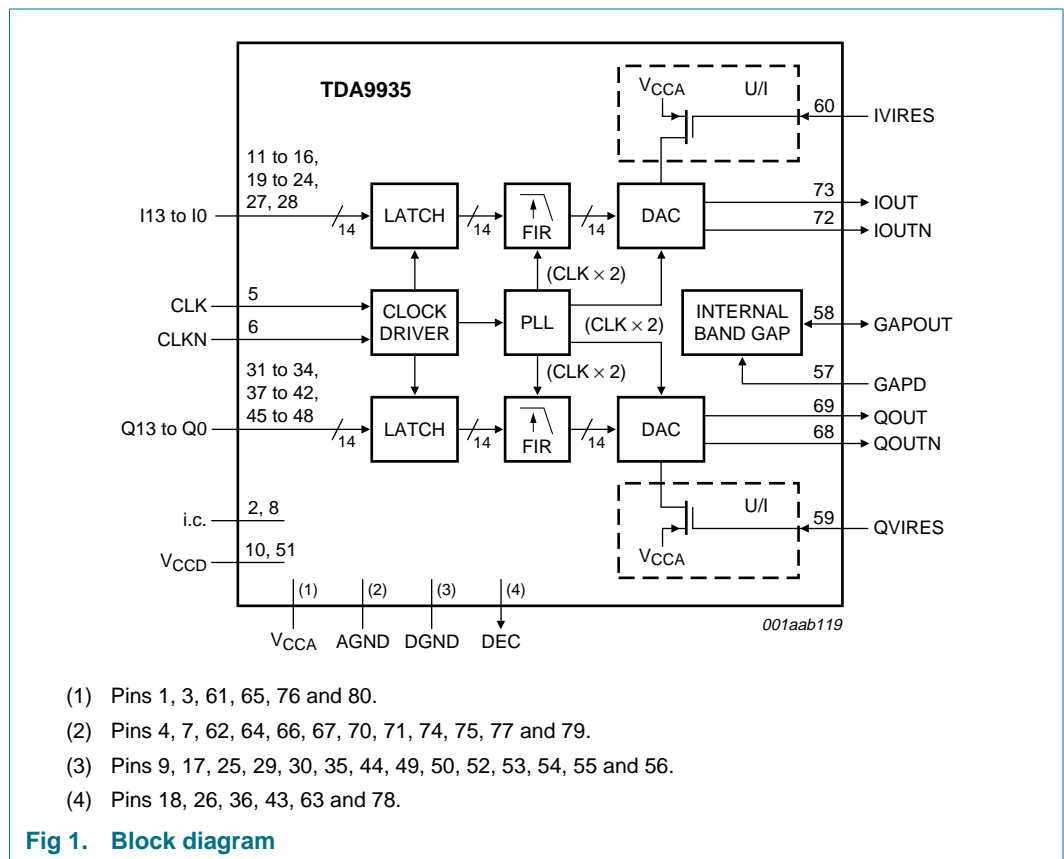
- Broadband wireless systems
- Digital radio links
- Cellular base stations
- Instrumentation

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
TDA9935HW	HTQFP80	plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad	SOT841-1

5. Block diagram



- (1) Pins 1, 3, 61, 65, 76 and 80.
- (2) Pins 4, 7, 62, 64, 66, 67, 70, 71, 74, 75, 77 and 79.
- (3) Pins 9, 17, 25, 29, 30, 35, 44, 49, 50, 52, 53, 54, 55 and 56.
- (4) Pins 18, 26, 36, 43, 63 and 78.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

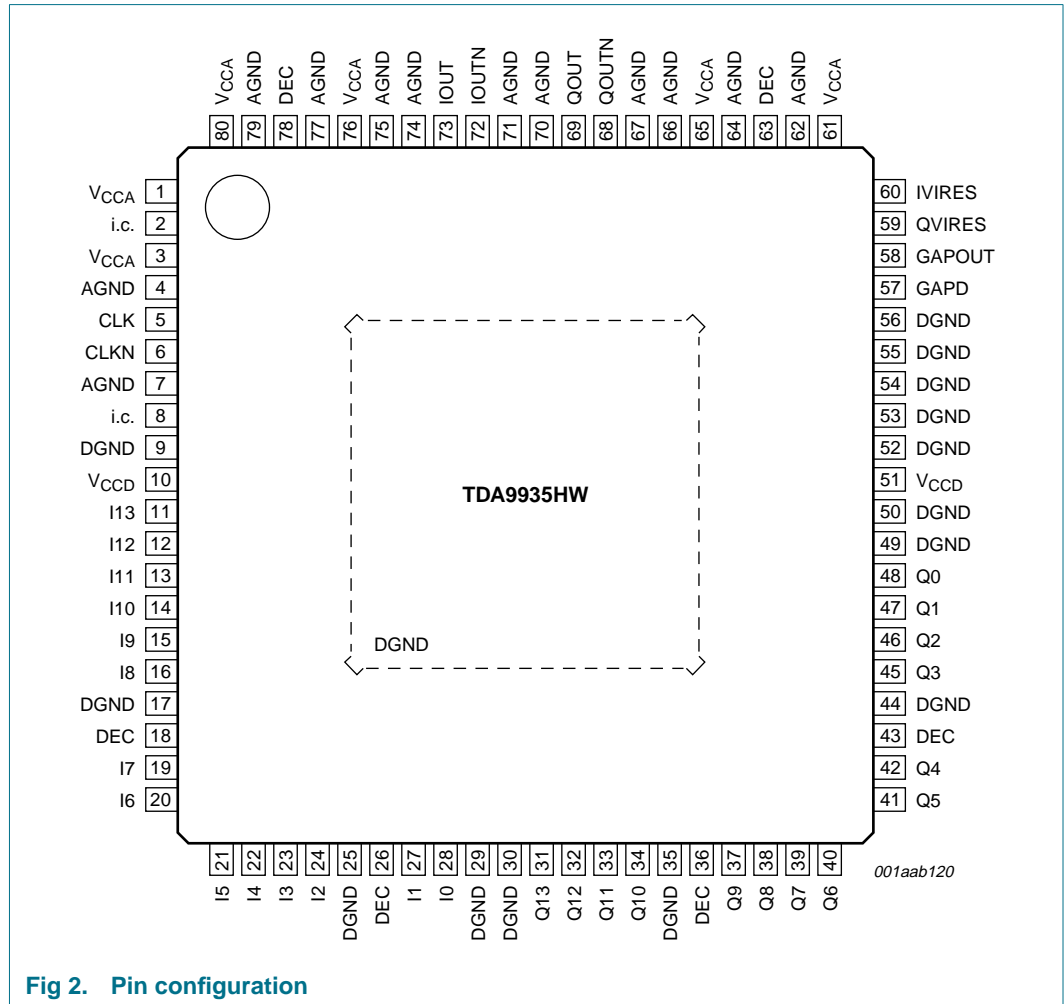


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type ^[1]	Description
V _{CCA}	1	S	analog supply voltage
i.c.	2	I/O	internally connected; leave open
V _{CCA}	3	S	analog supply voltage
AGND	4	G	analog ground
CLK	5	I	clock input
CLKN	6	I	complementary clock input
AGND	7	G	analog ground
i.c.	8	O	internally connected; leave open
DGND	9	G	digital ground

Table 2. Pin description ...continued

Symbol	Pin	Type ^[1]	Description
V _{CCD}	10	S	digital supply voltage
I13	11	I	I data input bit 13 (MSB)
I12	12	I	I data input bit 12
I11	13	I	I data input bit 11
I10	14	I	I data input bit 10
I9	15	I	I data input bit 9
I8	16	I	I data input bit 8
DGND	17	G	digital ground
DEC	18	O	decoupling node
I7	19	I	I data input bit 7
I6	20	I	I data input bit 6
I5	21	I	I data input bit 5
I4	22	I	I data input bit 4
I3	23	I	I data input bit 3
I2	24	I	I data input bit 2
DGND	25	G	digital ground
DEC	26	O	decoupling node
I1	27	I	I data input bit 1
I0	28	I	I data input bit 0 (LSB)
DGND	29	G	digital ground
DGND	30	G	digital ground
Q13	31	I	Q data input bit 13 (MSB)
Q12	32	I	Q data input bit 12
Q11	33	I	Q data input bit 11
Q10	34	I	Q data input bit 10
DGND	35	G	digital ground
DEC	36	O	decoupling node
Q9	37	I	Q data input bit 9
Q8	38	I	Q data input bit 8
Q7	39	I	Q data input bit 7
Q6	40	I	Q data input bit 6
Q5	41	I	Q data input bit 5
Q4	42	I	Q data input bit 4
DEC	43	O	decoupling node
DGND	44	G	digital ground
Q3	45	I	Q data input bit 3
Q2	46	I	Q data input bit 2
Q1	47	I	Q data input bit 1
Q0	48	I	Q data input bit 0
DGND	49	G	digital ground
DGND	50	G	digital ground

Table 2. Pin description ...continued

Symbol	Pin	Type ^[1]	Description
V _{CCD}	51	S	digital supply voltage
DGND	52	G	digital ground
DGND	53	G	digital ground
DGND	54	G	digital ground
DGND	55	G	digital ground
DGND	56	G	digital ground
GAPD	57	I	internal band gap power disable input
GAPOUT	58	I/O	band gap output voltage
QVIRES	59	I	Q DAC biasing resistor
IVIRES	60	I	I DAC biasing resistor
V _{CCA}	61	S	analog supply voltage
AGND	62	G	analog ground
DEC	63	O	decoupling node
AGND	64	G	analog ground
V _{CCA}	65	S	analog supply voltage
AGND	66	G	analog ground
AGND	67	G	analog ground
QOUTN	68	O	complementary Q DAC output current
QOUT	69	O	Q DAC output current
AGND	70	G	analog ground
AGND	71	G	analog ground
IOUTN	72	O	complementary I DAC output current
IOUT	73	O	I DAC output current
AGND	74	G	analog ground
AGND	75	G	analog ground
V _{CCA}	76	S	analog supply voltage
AGND	77	G	analog ground
DEC	78	O	decoupling node
AGND	79	G	analog ground
V _{CCA}	80	S	analog supply voltage

[1] Type description:
 S: Supply;
 G: Ground;
 I: Input;
 O: Output.

7. Functional description

The DAC is a segmented architecture composed of a 7-bit thermometer sub-DAC, and the remaining 7-bit in a binary weighted sub-DAC.

The device produces two complementary current outputs on both channels, respectively pins IOUT/IOUTN and QOUT/QOUTN which need to be connected via a load resistor to the ground.

Figure 3 shows the equivalent analog output circuit of one DAC, which consists of a parallel combination of PMOS current sources and associated switches for each segment.

The cascode source configuration enables to increase the output impedance of the source and set to improve the dynamic performance of the DAC by introducing less distortion.

Figure 4 shows the internal reference configuration. In this case the bias current is given by the output of the internal regulator connected to the inverting input of the internal operational amplifiers, while external resistors R_I and R_Q are connected respectively to pins IVIRES and QVIRES. Thus the output current of the two DACs is typically fixed to 20 mA with an appropriate choice of these resistors. This configuration is optimal for temperature drift compensation because the band gap can be matched with the voltage on the feedback resistors.

The relation between full-scale output current $I_{O(FS)}$ and the R_I (R_Q) is:

$$R_I = \frac{2048 \times V_{GAPOUT}}{82 \times I_{O(FS)}} \Omega$$

The output current can also be adjusted by imposing an external reference voltage to the inverting input pin GAPOUT and disabling the internal band gap with pin GAPD set to HIGH. At a voltage lower than 1.2 V the current can be set at values lower than 20 mA. The input references at pins IVIRES and QVIRES may also be driven by separate reference voltages to adjust independently the two DAC currents.

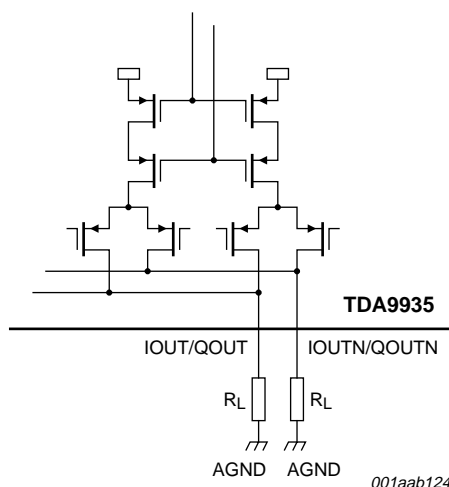


Fig 3. Equivalent analog output circuit

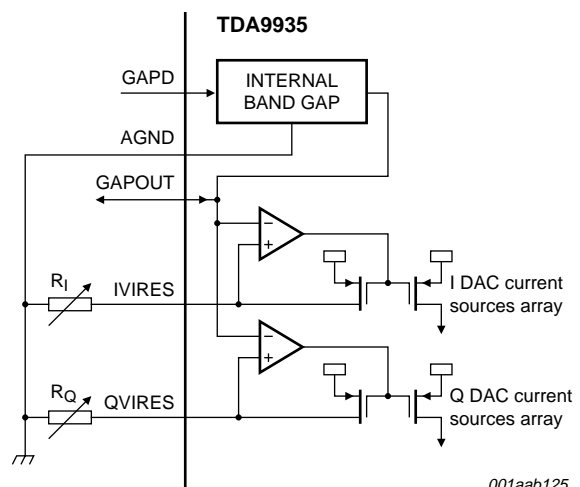


Fig 4. Internal reference configuration

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCD}	digital supply voltage		[1] -0.3	+3.9	V
V_{CCA}	analog supply voltage		[1] -0.3	+3.9	V
$\Delta V_{CCA-CCD}$	supply voltage difference between the analog and digital supply voltages		-150	+150	mV
V_I	voltage at input pins	pins Qn and In referenced to DGND	-0.3	$V_{CCD} + 0.3$	V
		pins IVIRES, QVIRES and GAPD referenced to AGND	-0.3	$V_{CCA} + 0.3$	V
		pins CLK and CLKN referenced to AGND	-0.3	$V_{CCA} + 0.3$	V
V_O	voltage at output pins	pins IOUT, IOUTN, QOUT and QOUTN referenced to AGND	-0.3	$V_{CCA} + 0.3$	V
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
T_j	junction temperature		-	125	°C

[1] All supplies are connected together.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	27.1	K/W
$R_{th(c-a)}$	thermal resistance from case to ambient	in free air	11.8	K/W

10. Characteristics

Table 5. Characteristics

$V_{CCD} = V_{CCA} = 3.0\text{ V to }3.6\text{ V}$; AGND and DGND connected together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{CCD} = V_{CCA} = 3.3\text{ V}$, $I_{O(FS)} = 20\text{ mA}$ and $T_{amb} = 25\text{ °C}$; dynamic parameters measured using output schematic given in [Figure 10](#); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCD}	digital supply voltage		3.0	3.3	3.6	V
V_{CCA}	analog supply voltage		3.0	3.3	3.6	V
I_{CCD}	digital supply current		-	55	65	mA
I_{CCA}	analog supply current		-	73	85	mA
P_{tot}	total power dissipation	$f_{CLK} = 80\text{ Msample/s}$; $f_{IOUT} = f_{QOUT} = 5\text{ MHz}$	-	422	540	mW
Clock inputs (CLK and CLKN)						
$V_{I(CM)}$	common mode input voltage		-	1.65	-	V
ΔV_{CLK}	differential input voltage swing		-	1.0	-	V
Analog outputs (IOUT, IOUTN, QOUT and QOUTN)						
$I_{O(FS)}$	full-scale output current	differential outputs	4	-	20	mA
R_o	output resistance		[1] -	150	-	k Ω
C_o	output capacitance		[1] -	3	-	pF
Digital inputs (I0 to I13, Q0 to Q13 and GAPD)						
V_{IL}	LOW-level input voltage		DGND	-	$0.3V_{CCD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CCD}$	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.3V_{CCD}$	-	5	-	μA
I_{IH}	HIGH-level input current	$V_{IH} = 0.7V_{CCD}$	-	5	-	μA
Reference voltage output (GAPOUT)						
V_{GAPOUT}	output voltage		-	1.31	-	V
I_{GAPOUT}	output current	external voltage	-	1	-	μA
ΔV_{GAPOUT}	output voltage drift		-	± 133	-	ppm/ $^{\circ}\text{C}$
Clock timing inputs (CLK and CLKN)						
$f_{CLK(max)}$	maximum clock rate		80	-	-	Msample/s
$t_{W(CLKH)}$	clock HIGH pulse width		5	-	-	ns
$t_{W(CLKL)}$	clock LOW pulse width		5	-	-	ns
Input timing (I0 to I13 and Q0 to Q13); see Figure 5						
$t_{h(i)}$	input hold time		1.1	-	3.4	ns
$t_{su(i)}$	input setup time		-1.5	-	+0.7	ns

Table 5. Characteristics ...continued

$V_{CCD} = V_{CCA} = 3.0\text{ V to }3.6\text{ V}$; AGND and DGND connected together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{CCD} = V_{CCA} = 3.3\text{ V}$, $I_{O(FS)} = 20\text{ mA}$ and $T_{amb} = 25\text{ °C}$; dynamic parameters measured using output schematic given in [Figure 10](#); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital filter specification (FIR); see Figure 6, Figure 7 and Table 7						
N	order		-	42	-	
$f_{I(D)}$	data input rate		80	-	-	Msample/s
R_{PBW}	ripple in pass bandwidth	f_{data}/f_{CLK} ; 0.005 dB attenuation	-	0.405	-	
PBW	pass bandwidth	f_{data}/f_{CLK} ; 3 dB attenuation	-	0.479	-	
SBR	stop band rejection	$f_{data}/f_{CLK} = 0.6\text{ to }1$	-	69	-	dB
$t_{d(g)}$	group delay time		-	$11T_{CLK}$	-	ns
Analog signal processing						
INL	integral non-linearity		-	± 2.9	-	LSB
DNL	differential non-linearity		-	± 1.5	-	LSB
$I_{n(o)}$	output noise current		-	120	-	$\mu A/\sqrt{Hz}$
$E_{offset(o)}$	output offset error	relative to full scale	-	-0.3	-	%
E_G	gain error	relative to full scale	-5.4	-	+5.4	%
M_G	gain matching	between I and Q, relative to full scale	-	± 0.2	-	%
SFDR	spurious-free dynamic range	$f_{CLK} = 80\text{ Msample/s}$; BW = Nyquist				
		$f_{OUT} = 2.5\text{ MHz at }0\text{ dBFS}$	-	80	-	dBc
		$f_{OUT} = 5\text{ MHz at }0\text{ dBFS}$	-	72	-	dBc
		$f_{OUT} = 13\text{ MHz at }0\text{ dBFS}$	-	64	-	dBc
H2	second harmonic	$f_{OUT} = 5\text{ MHz}$	-	73	-	dBc
		$f_{OUT} = 13\text{ MHz}$	-	65	-	dBc
H3	third harmonic	$f_{OUT} = 5\text{ MHz}$	-	88	-	dBc
		$f_{OUT} = 13\text{ MHz}$	-	86	-	dBc
IMD2	second order two-tone intermodulation rejection	$f_{CLK} = 80\text{ Msample/s}$; $f_{OUT1} = 10\text{ MHz}$; $f_{OUT2} = 12\text{ MHz}$; BW = Nyquist	-	65	-	dBc
IMD3	third order two-tone intermodulation rejection	$f_{CLK} = 80\text{ Msample/s}$; $f_{OUT1} = 10\text{ MHz}$; $f_{OUT2} = 12\text{ MHz}$	-	84	-	dBc
THD	total harmonic distortion	$f_{CLK} = 80\text{ Msample/s}$; BW = Nyquist				
		$f_{OUT} = 2.5\text{ MHz}$	-	75	-	dBc
		$f_{OUT} = 5\text{ MHz } (T_{amb} = 25\text{ °C})$	68	71	-	dBc
NSD	noise spectral density	$f_{CLK} = 80\text{ Msample/s}$				
		$f_{OUT} = 2.5\text{ MHz}$	-	-155	-	dBm/Hz
		$f_{OUT} = 5\text{ MHz}$	-	-155	-	dBm/Hz
		$f_{OUT} = 19\text{ MHz}$	-	-153	-	dBm/Hz

Table 5. Characteristics ...continued

$V_{CCD} = V_{CCA} = 3.0\text{ V to }3.6\text{ V}$; AGND and DGND connected together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{CCD} = V_{CCA} = 3.3\text{ V}$, $I_{O(FS)} = 20\text{ mA}$ and $T_{amb} = 25\text{ °C}$; dynamic parameters measured using output schematic given in Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S/N	signal-to-noise ratio	$f_{CLK} = 80\text{ Msample/s}$; $BW = \text{Nyquist}$				
		$f_{OUT} = 2.5\text{ MHz}$	-	80	-	dBc
		$f_{OUT} = 5\text{ MHz}$	70	80	-	dBc
		$f_{OUT} = 19\text{ MHz}$	-	78	-	dBc
ACPR	adjacent channel power ratio	baseband; 5 MHz channel spacing; $BW = 3.4\text{ MHz}$				
		$f_{OUT} = 2.5\text{ MHz}$	-	69	-	dBc
		$f_{OUT} = 20\text{ MHz}$	-	71	-	dBc

[1] Guaranteed by design.

Table 6. Band gap

Band gap disable (GAPD)	Band gap input/output (GAPOUT)	Internal band gap
LOW	output ($V_{GAPOUT} = 1.2\text{ V}$)	enable
HIGH	input	disable

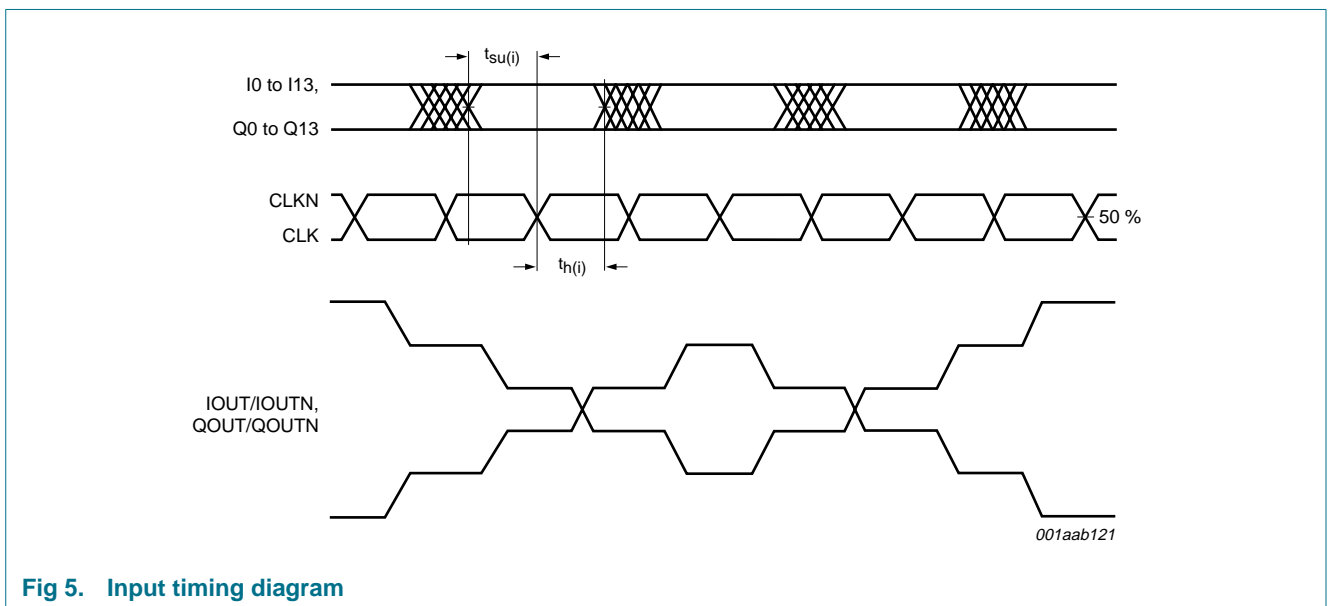


Fig 5. Input timing diagram

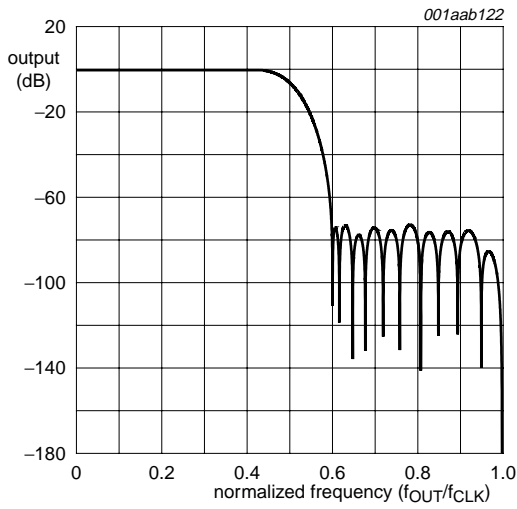


Fig 6. FIR filter frequency response

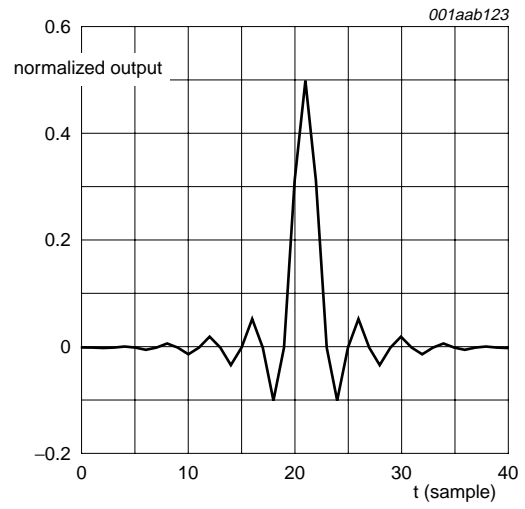


Fig 7. FIR filter impulse response

Table 7. Interpolation FIR filter coefficient

Coefficient	Coefficient	Value
H(1)	H(43)	10
H(2)	H(42)	0
H(3)	H(41)	-31
H(4)	H(40)	0
H(5)	H(39)	69
H(6)	H(38)	0
H(7)	H(37)	-138
H(8)	H(36)	0
H(9)	H(35)	248
H(10)	H(34)	0
H(11)	H(33)	-419
H(12)	H(32)	0
H(13)	H(31)	678
H(14)	H(30)	0
H(15)	H(29)	-1083
H(16)	H(28)	0
H(17)	H(27)	1776
H(18)	H(26)	0
H(19)	H(25)	-3282
H(20)	H(24)	0
H(21)	H(23)	10364
H(22)	-	16384

11. Application information

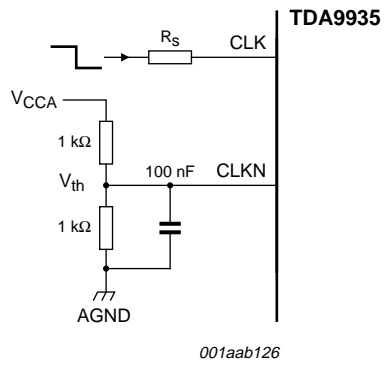


Fig 8. Single-ended clock schematic

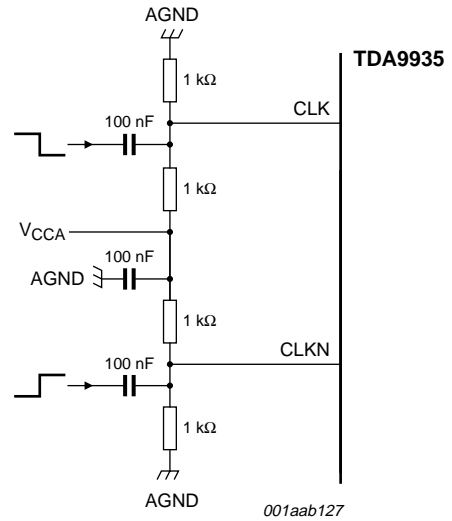
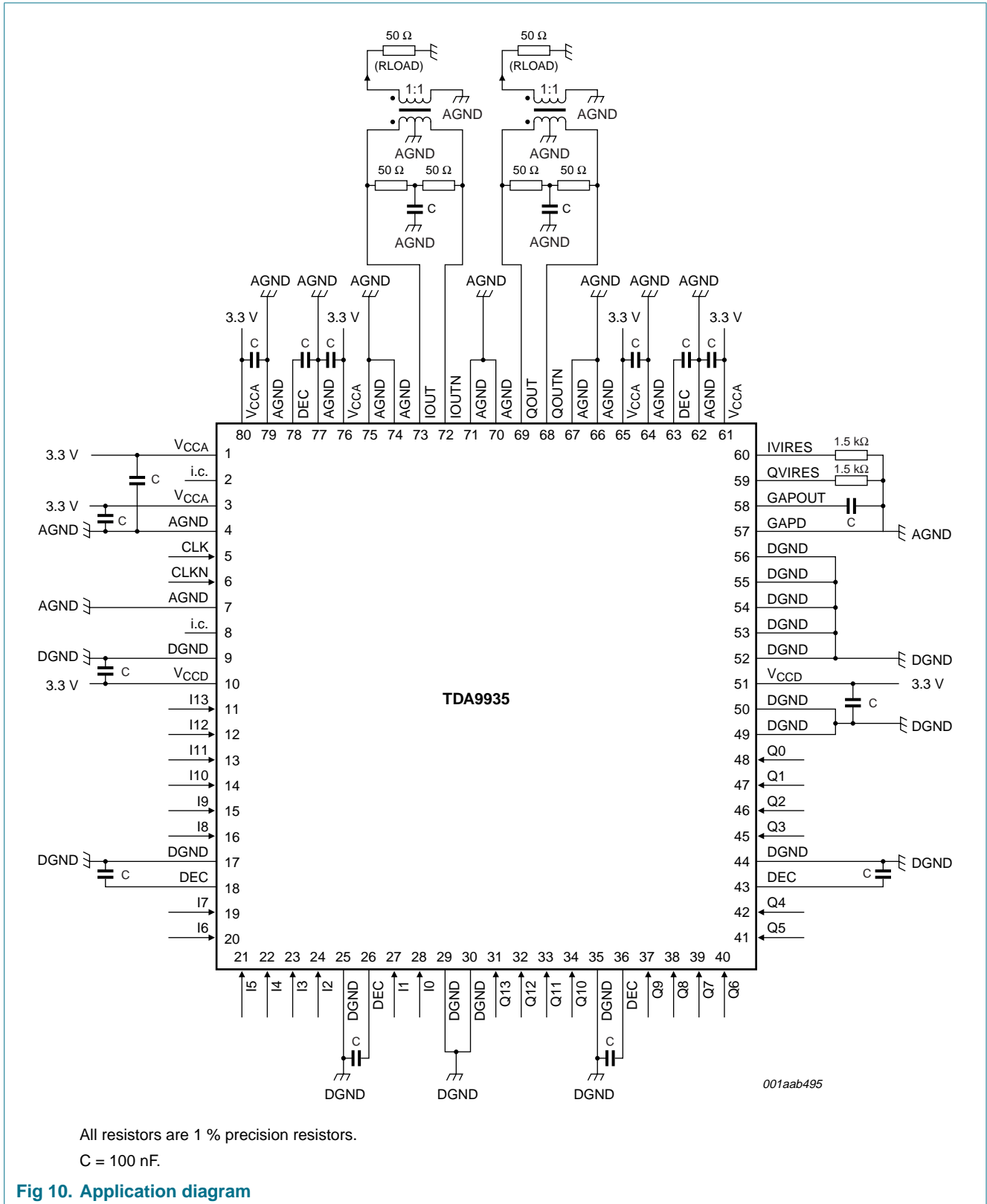


Fig 9. Differential clock schematic



12. Package outline

HTQFP80: plastic thermal enhanced thin quad flat package; 80 leads; body 12 x 12 x 1 mm; exposed die pad SOT841-1

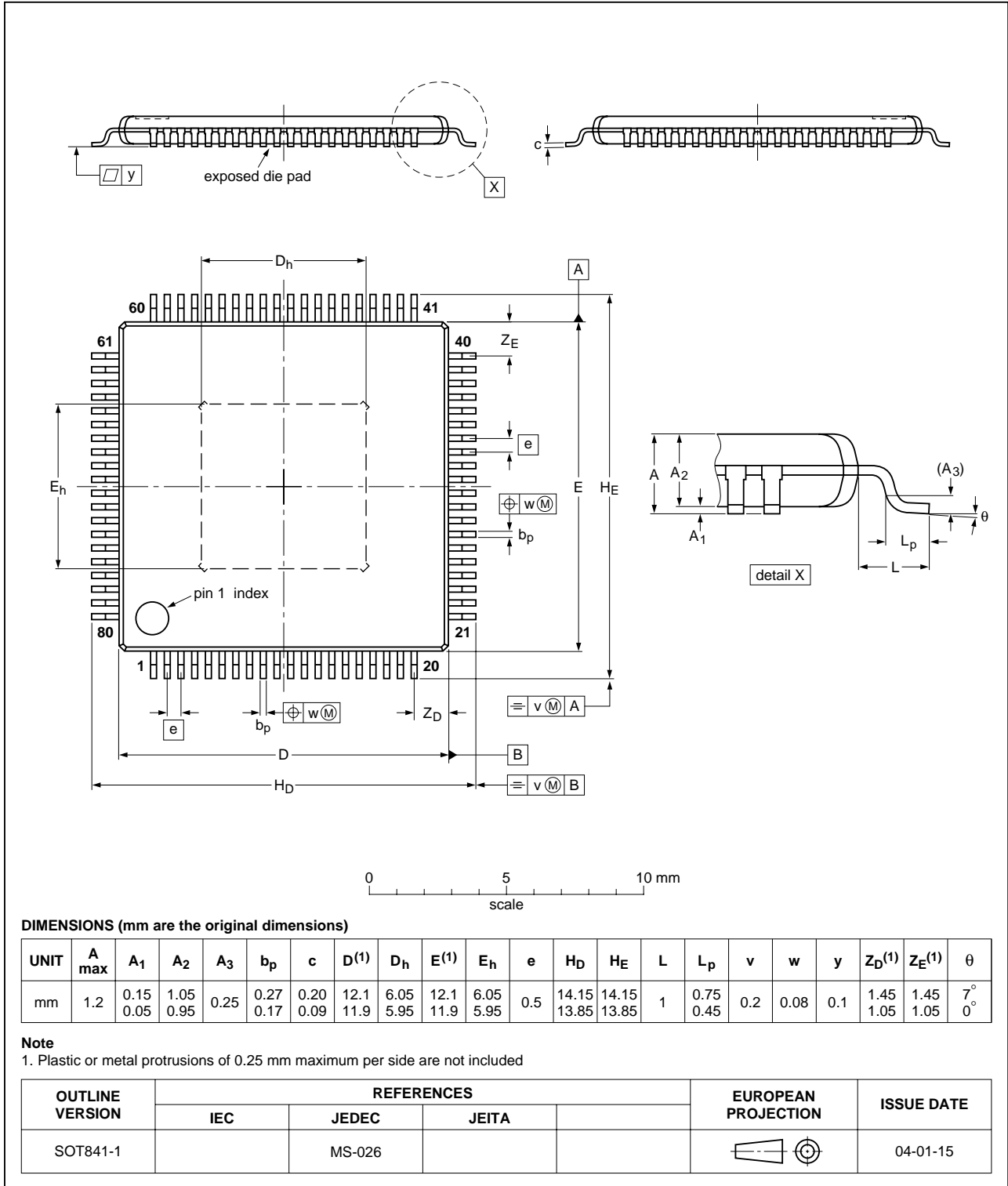


Fig 11. Package outline SOT841-1 (HTQFP80)

13. Abbreviations

Table 8. Abbreviations

Acronym	Description
BW	BandWidth
BWA	Broadband Wireless Access
CDMA	Code Division Multiple Access
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
IF	Intermediate Frequency
LMDS	Local Multipoint Distribution Service
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-Locked Loop
PMOS	Positive-Metal Oxide Semiconductor
SFDR	Spurious-Free Dynamic Range
WCDMA	Wideband Code Division Multiple Access
WLL	Wireless Local Loop

14. Glossary

14.1 Static parameters

DNL — Differential Non-Linearity. The difference between the ideal and the measured output value between successive DAC codes.

INL — Integral Non-Linearity. The deviation of the transfer function from a best-fit straight line (linear regression computation).

14.2 Dynamic parameters

IMD2 — Two-tone InterModulation Distortion rejection; Second order. From a dual-tone digital input sine wave (these two frequencies are close together), the intermodulation distortion product IMD2 is the ratio of the RMS value of either tone and the RMS value of the worst 2nd-order intermodulation product.

IMD3 — Two-tone InterModulation Distortion rejection; Third order. From a dual-tone digital input sine wave (these two frequencies are close together), the intermodulation distortion product IMD3 is the ratio of the RMS value of either tone and the RMS value of the worst 3rd-order intermodulation product.

SFDR — Spurious-Free Dynamic Range. The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

S/N — Signal-to-Noise ratio. The ratio of the RMS value of the reconstructed output sine wave to the RMS value of the noise excluding the harmonics and the DC component.

THD — Total Harmonic Distortion. The ratio of the RMS value of the harmonics of the output frequency to the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

15. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9935_4	20070917	Product data sheet	-	TDA9935_3
Modifications:	<ul style="list-style-type: none"> Amended the (alternative) descriptive title 			
TDA9935_3	20070611	Product data sheet	-	TDA9935_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Extended abbreviations list in Section 13. 			
TDA9935_2	20060809	Preliminary data sheet	-	TDA9935_1
TDA9935_1 (9397 750 13346)	20041214	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features	1
3	Applications	1
4	Ordering information	2
5	Block diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	6
8	Limiting values	7
9	Thermal characteristics	7
10	Characteristics	8
11	Application information	12
12	Package outline	14
13	Abbreviations	15
14	Glossary	15
14.1	Static parameters	15
14.2	Dynamic parameters	15
15	Revision history	16
16	Legal information	17
16.1	Data sheet status	17
16.2	Definitions	17
16.3	Disclaimers	17
16.4	Trademarks	17
17	Contact information	17
18	Contents	18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 September 2007

Document identifier: TDA9935_4